a liquid crystal layer being interposed between the first insulating substrate and the second insulating substrate;

a plurality of gate wiring lines, each of which is formed on the first insulating substrate and transmits a scanning signal;

a gate insulating film being formed on the first insulating substrate and the plurality of gate wiring lines;

a plurality of drain wiring lines, each of which is formed on the gate insulating film and transmits a video signal;

a plurality of semiconductor layers being formed on the gate insulating film and at least under one of the plurality of drain wiring lines;

thin film transistor sections provided for respective pixels, each of the thin film transistor sections has a semiconductor channel layer formed of a part of one of the plurality of semiconductor layers extended at least over a part of one of the plurality of gate wiring lines, a drain electrode formed of a part of the one of the plurality of drain wiring lines situated on the semiconductor channel layer, a source electrode formed on the semiconductor channel layer at an opposite side of the part of the one of the plurality of gate wiring lines to the drain electrode to be spaced from the drain electrode; and

a protective film covering the plurality of drain wiring lines, the source electrodes, and the drain electrodes, wherein

each of the respective pixels has a pixel electrode formed on the protective film and contacted with the source electrode of one of the thin film transistor sections through a first contact hole perforating the protective film and a charge-holding capacitance section having an upper electrode connected to one of the pixel electrode through a second contact hole perforating the protective film and a lower electrodes formed of another of the plurality of the gate wiring line or a material thereof,

a dielectric film being interposed between the lower electrode and the upper electrode of the charges-holding capacitance section includes at least the gate insulating film, and

the charges-holding capacitance section is provided with another of the plurality of semiconductor layers having a planar outline inside which the second contact hole is located and being contact with the pixel electrode.

3. A liquid crystal display device according to claim 2, wherein the second contact hole perforates the another of the plurality of the semiconductor layer also at the charges-holding capacitance section, and the pixel electrode contacts with the gate insulating film through the second contact hole.

4. A liquid crystal display device according to claim 3, wherein the another of the semiconductor layers is formed around the second contact hole on the gate insulating film.

Please add new claim 22 as follows:

22. A liquid crystal display device according to claim 2, wherein the dielectric film Interposed between the lower electrode and the upper electrode at the charges-holding capacitance section also includes the another of the semiconductor layers.